Reviewer 1:

* For the latches tested, the magnitude of the pulse (and by default the injected charge) does not have a direct correlation on the latch’s ability to tolerate an error. For all latches tested, a pulse will not be stored in the storage loop no matter the pulse size. Specifically, the presented latches that are SEU tolerant will not upset unless two nodes have simultaneous pulses. DNU tolerant latches will not upset unless three nodes have simultaneous pulses and TNU tolerant latches will not upset unless four nodes have simultaneous pulses. This is clarified in the last paragraph of the Section 3.
* Similar to the above concern, the latches do not have a critical charge in the conventional sense as the number of pulses, not the magnitude, contribute to the ability of the latch to tolerate a pulse. However, this does lead to a single corner case where the output could be upset with such high energy that the output is not able to recover before the end of the transparent mode. This is discussed in section 5 paragraph 2. We tried to characterize the corner case for charges of up to 1 nC and found that the case did not occur. Larger charge values were tested however HSPICE would not converge on a solution.
* Table 1 has been amended such that the “Delay” entry is the D->Q delay
* Setup and hold times are typically characterized for flip-flops and the design of hardened flip-flops are beyond the scope of this paper. It is of belief of the author that the D->Q delay is sufficient to judge the performance and suitability of both conventional and proposed latch designs. Specifically, the latches are set when the CLK is set to high which puts the latch in transparent mode. The value stored in the latch is that which is on the input when the CLK (or commonly referred to as the Enable) moves to a low value. In this case, the only timing constraint is that the overlap between the input data (D) and the CLK is equal to or greater than the propagation delay of the latch.
* I have made the lines thicker for Fig. 21 (previously Fig. 19) so they should be more visible.

Reviewer 2:

* The title was changed to: Radiation Hardened Latch Designs for Double and Triple Node Upsets

Reviewer 3:

* Section 2 Paragraph 1: DNUCS is changed to DNCS and the acronym is defined.
* Section 2 Paragraph 3: HSMUF acronym was not defined because its definition was not given in the reference. The figure for this latch was already in the paper but a reference to the figure was placed in the first sentence.
* Section 2 Paragraph 4: The DONUT latch acronym was defined
* Fig 5: INP changed to INPUT to clarify that the pin is an input
* Fig. 2 and Fig. 3: Both figures give schematic of the DNCS latch. In section 2 paragraph 1, the figure is referenced.
* Section 3 Paragraph 5: The last sentence of the paragraph quotes the schematic.
* Section 4 Paragraph 1: The word tedious was changed to difficult. The sentence as a whole had awkward wording which was addressed.
* Section 1 Paragraph 7: A citation to the previous paper is added in the first sentence.

That paper has been proofread and any remaining typos that were found were fixed.